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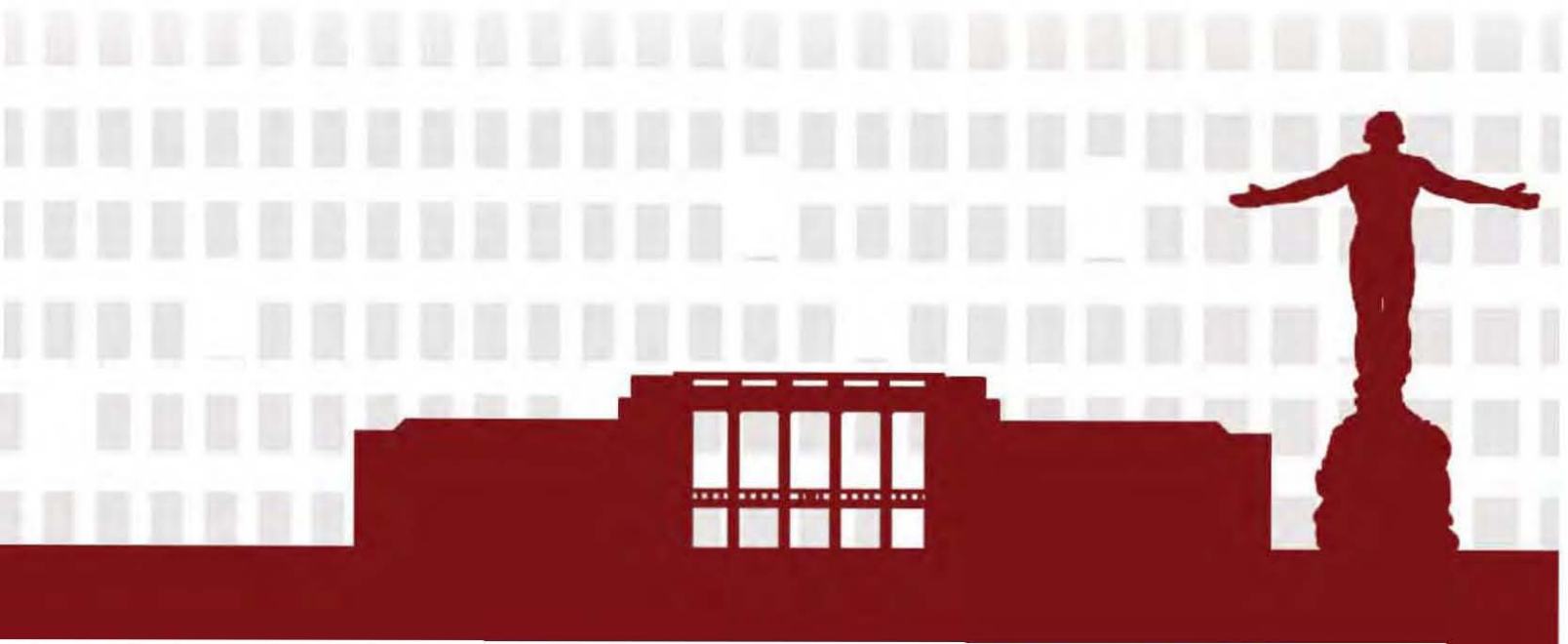
Metro Manila, Philippines



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LOW POWER AND PVT RESILIENT 2.4GHz RF FRONT-END RECEIVER FOR RF POWERED WIRELESS SENSOR NODES

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ABSTRACT

In today's world, the demand for easier and faster access to information such as for health monitoring, environmental awareness, and power line monitoring have led to the development of wireless sensor nodes (WSN). Reliable data communication is the key to the efficient data flow and system monitoring. With this, the receiver block need to operate efficiently across changes in the environment, power supply voltage, and especially with respect to its process variations.

From preliminary characterization results, PVT variations caused 5dB change in transistor gain and to its noise figure, consequently, affecting the signal to noise ratio (SNR) with the same amount. To this extent, the variations must be mitigated as much as possible to ensure the reliability of the data flow.

However, with the existing methodologies to mitigate the PVT variations in the literature, they do not meet the power constraints and the robustness required for an energy harvested powered sensor node. Variable gain amplifiers with tunable input matching, off chip frequency reference blocks and scalable supply voltage introduce area overhead and more complex blocks lead to overhead power consumption and prone to more variations making them not suitable for the requirements of an integrated RF powered sensor node. Also, overdesigning the specifications of the front end receiver is not an option because of overhead in power consumption.

The aim of this research is to develop a design methodology that will identify the system and circuit level non-idealities of receiver front end blocks which are de-pendent on process, voltage and temperature variations. In addition, techniques to reduce these variations on a fully integrated WSN will be explored. The chip will be implemented in a 65nm CMOS process with a data operating frequency of 2.4GHz, 1 Mbps data rate, BER of 10e-3 and temperature range from 0 to 100 degrees Celsius. 2

Shown in Figure 1 is the block diagram of the front end receiver which is composed of three main blocks namely: bandpass filter, low noise amplifier, and mixer.

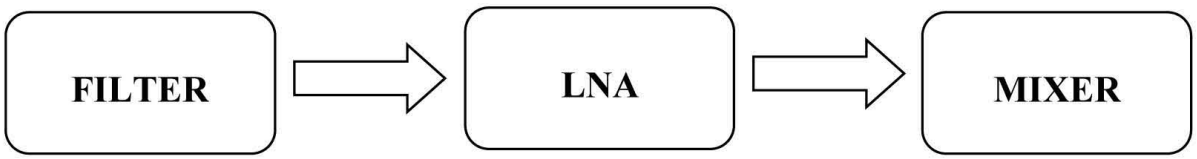

Figure 1. Front-end receiver block diagram

In the design implementation of these blocks, the simplest yet reasonable topology is used to lessen the effect of variations contributed by the transistor devices. For the low noise amplifier, a cascode topology with resistive shunt feedback is chosen to attain both the required gain and area constraint. As for the mixer, a passive type single balanced mixer is implemented due to limitation in power consumption.

And to further mitigate the variations suitable for the requirements of an integrated WSN, a constant transconductance bias topology is employed on the amplifier, shifting the burden on the DC level rather than on the higher frequency of operation to compensate the constraints in power budget.

Simulations of the designed front end receiver in schematic level (Table 1) present almost 2dB SNR change across PVT variations. Further testing and optimization of blocks will still be done on this research work.

PARAMETERS	SS 100	FF00	TT27
Gain (dB)	14.8	13.5	14.4
SNR (dB)	19.7	17.9	19.1
Power (uW)	884	870	875

Table 1. Summary of results of the front end receiver across PVT variations

Keywords: 2.4GHz low noise amplifier passive mixer, constant gm bias, RF receiver

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